REMARKS

The Examiner Lynne Ann Gurley is thanked for carefully examining and reviewing the subject patent application. The specification and claims have been reviewed and both the specification and the claims have been amended in accordance with all of the Examiner's kind suggestions. The specification has been reviewed by the Applicants and appears to be acceptable.

The Examiner's Final restriction requirement is acknowledged, and non-elected claims 31 and 32 have been cancelled, in a prior action. Applicant reserves the right to file a Divisional application at a later date.

All claims 1 through 30 are now believed to be in allowable condition, and allowance is so requested.

SUMMARY OF INVENTION

A method is described whereby trench openings in dual damascene trench and via etch processes are formed by using a two component hard mask layer, termed a bi-layer, over different intermetal dielectrics, IMD. This method solves dual damascene patterning problems, such as, fencing and sub-trench formation. Via first patterning in dual damascene processing is one of the major integration schemes for copper backend of line (BEOL) integration. Via first dual damascene scheme usually uses a hard mask layer deposited on top of an inter-metal dielectric (IMD) film stack. The dual damascene trench etch requires uniform trench depth across wafer after etch. In addition, via top corner profiles need to be well maintained without any fencing or faceting. These problems and drawbacks were difficult to detect. The present method solves these problems by using a two component hard mask layer, termed a bi-layer, deposited directly on top of an inter-metal dielectric (IMD) film stack. The Applicants discovered

these problems and the Applicants' claimed invention uniquely solved these fencing and faceting problems.

CLAIM REJECTIONS - 35 U.S.C. 103(a):

Reconsideration of the rejection of Claims 1 - 30, under 35 U.S.C. 103(a), as being unpatentable over Weidman et al. (US 2003/0176058, dated 9/18/03, filed 3/18/02), is requested, based on the following.

In the Applicants claimed invention, independent claim 1 is broad and general claim to lay the foundation for outlining the processing method whereby via and trench openings are formed in a dual damascene process utilizing a bi-layered hard mask for patterning and etching steps. It features a via opening first, with subsequent trench formation. The dependent claims 2, 3, and 4, follow with addition general, broad background claim information, adding to the independent claim 1. Claim 1 has been amended to better define and limit the Applicant's claimed invention, being more specific in description of the bi-layered hard mask, thereby circumventing the prior art descriptions of Weidman's Figs. 1A-1H. In fact, Weidman's prior art description

appears to be the same general process that Weidman subsequently discloses and claims in Weidman's claim 1.

Another patentable difference, now found in the Applicant's amended claim 1, from art descriptions of Weidman's Figs. 1A-1H, is that the bi-layered hard mask is: USG, undoped silicate glass, SiC or SiN.

Weidman does not teach or suggest the Applicant's claimed invention, and there are patentable differences from Weidman. The key points of the Applicant's claimed invention are: a) the detailed processing steps disclosed, descriptions, and claims, b) the differences in the materials disclosed, c) the explicit teaching of the process parameters include layer thickness ranges. Supporting the above, reference Applicant's claim 5, (partially modified into claim 4), which discloses bi-layered hard mask material of USG / SiC or SiN, with thickness ranges and various insulating IMD dielectric material and thick range (amended into claim 4). Nor does Wiedman teach or suggest the set of etch step disclosed by Applicant in claim 7, for example.

There is a wide range of dielectric insulating material, IMD, disclosed by the Applicant, see amended

claims 5 and 4, for example, doped F and undoped oxides, carbon doped oxide, organic based low-k dielectric, and porous low-k dielectric, which are not all found in Weidman.

The inclusion of dual damascene processing of the copper metallurgy by the Applicant in Figs. 2E and 2F is essential to complete the processing method, and the Applicant's claimed invention would be found incomplete without this aspect in the description of the method.

Furthermore, the dual damascene trench etch requires uniform trench depth across wafer after etch. In addition, via top corner profiles need to be well maintained without any fencing or faceting. These problems and drawbacks were difficult to detect. The present method solves these problems by using a two component hard mask layer, termed a bi-layer, deposited directly on top of an inter-metal dielectric (IMD) film stack. The Applicants discovered these problems and the Applicants' claimed invention uniquely solved these fencing and faceting problems.

A key point and a nontrivial point is that Weidman's disclosure lacks a fair number of key elements, namely:

a) not explicitly teaching that the BARC is formed with photoresist, a convenient material

b) the via is filled with photoresist, a convenient process

c) fails to specify layer thickness

d) fails to teach some of the IMD/hard mask stacks

e) fails to disclose key etching formulae

f) fails to teach repeating processing steps to form multiple layers of interconnects

g) fails to teach dual damascene processing with Cu seed layer in trench and via openings, and forming excess Cu, and then planarizing the excess Cu

h) fails to disclose applications for MOSFET, CMOS, in memory and logic devices

Using the Applicant's claimed invention with BARC and fill layers both made of photoresist, is clever and Wiedman neither teaches nor suggests this approach.

Concerning the obviousness of the Applicant's claimed invention "to one skilled in the art", the Examiner demonstrates a type of impermissible hindsight,

by recognizing the advisability to combine the prior art reference of Weidman only after the Applicants have claimed their processing combinations.

FINAL REMARKS

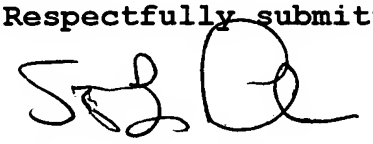
The Examiner Lynne Ann Gurley is thanked again for carefully examining and reviewing the subject patent application. The claims and specification have been reviewed and both the specification and the claims have been amended in accordance with the Examiner's kind suggestions.

All rejected claims 1 through 30 are believed to be in allowable condition, and allowance is so requested.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

It is requested that should there be any problems with this Amendment, please call the undersigned Attorney at (845) 452-5863.

Respectfully submitted,



Stephen B. Ackerman,
Reg. No. 37,761